

## VOLTAGE PROFILE ENHANCEMENT IN A POWER SYSTEM BASED ON SVC CONTROL STRATEGY USING PSIM SOFTWARE

K. S. RAMANJANEYULU<sup>1</sup> & K. PADMA<sup>2</sup>

<sup>1</sup>M.E. Scholar, Department of EEE, Andhra University, Visakhapatnam, Andhra Pradesh, India

<sup>2</sup>Assistant Professor, Department of EEE, Andhra University, Visakhapatnam, Andhra Pradesh, India

### ABSTRACT

The objective of this paper is to keep the power system to remain in voltage stable condition when it experiences a load change and contingency, also deals with the simulation of various FACTS controllers using simulation with PSIM simple circuit model of SVC Control Strategy system was simulated. This paper explains about the simulation and implementation of thyristor controlled reactor and thyristor switched capacitor of SVC. An SVC can control the voltage magnitude at the end of power transmission line under the conditions of load changing at the end of transmission line and changing in voltage magnitude at the voltage source at the other end of the line. The SVC system is simulated using PSIM and the simulation results are presented graphically. The power and control circuits are simulated. The current drawn by the SVC varies with the variation in the firing angle. The experimental results are given with the simulation results.

**KEYWORDS:** Static VAR Compensator, Thyristor Controlled Reactor, Thyristor Switched Capacitor, PSIM Software

### INTRODUCTION

The load is always changing and is normally unbalanced in a distribution system. System unbalance will increase losses and may cause adverse effects on industrial machines and generators. Unlike traditional shunt reactive elements, a static var compensator (SVC) is able to rapidly and smoothly supply or absorb reactive power by controlling the firing delay angles of thyristors. They have been used in transmission and distribution systems for voltage and reactive power control [1],[2]. When the power system operates under heavy loading conditions, the voltage drops at certain buses could involve voltage instability[3]. This instability can result in generation tripping which also cause system breakdown. The voltage stability problem may become more and more frequent in the deregulated electricity market where power needs to flow in directions opposite to those foreseen at the design stage [4, 8]. To obtain secure operating conditions, sufficient reactive powers have to be foreseen at various buses, controlling reactive powers according to voltage stability criteria[10, 7]. Recently, power electronics development and nonlinear control theory have involved the real application of structural control of power systems. FACTS devices, such as Static Var.

Compensators, unified power flow controllers, thyristor series capacitors etc, are used to dynamically adjust the network configuration to enhance steady state performance as well as system stability. FACTS controllers can be easily driven and inherently have no inertia hence, speed of control is their potential performance advantage. The application of FACTS technology can counteract voltage instability, allowing system capability to increase significantly, thus maintaining bus bar voltages around their nominal values [5, 6, 9]. In this paper, a new control strategy of SVC for increasing voltage stability in power distribution system is introduced. For this purpose, a practical system is described and

the solution method is proposed at the end. The proposed control method of SVC is simulated on practical system with PSIM software.

### Static VAR Compensator (SVC)

Static VAR systems are applied by utilities in transmission applications for several purposes. The primary purpose is usually for rapid control of voltage at weak points in a network. Installations may be at the midpoint of transmission interconnections or at the line ends. Static VAR Compensators are shunting connected static generators / absorbers whose outputs are varied so as to control voltage of the electric power systems [11]. In its simple form, SVC is connected as Fixed Capacitor-Thyristor Controlled. The SVC is connected to a coupling transformer that is connected directly to the ac bus whose voltage is to be regulated. The basic SVC schemes are: Thyristor controlled reactor and fixed capacitor, TCR/FC, Thyristor switched capacitor, TSC, Thyristor controlled reactor/Thyristor switched capacitor, TCR/TSC.

The SVC regulates voltage at its terminals by controlling the amount of reactive power injected into or absorbed from the power system. When system voltage is low, the SVC generates reactive power (SVC capacitive). When system voltage is high, it absorbs reactive power (SVC inductive). SVC principle is supplying a varying amount of leading or lagging VAR to the lagging or leading system. The reactor power of SVC is:

$$Q_{SVC} = \frac{E^2(X_C[2\pi - \alpha + \sin 2\alpha] - \pi X_L)}{\pi X_C X_L} \quad (1)$$

Generally, by changing the firing angle ' $\alpha$ ' the fundamental reactance  $X_L$  of the reactor is changed. Conventional thyristor controlled compensator, the SVC, presents variable reactive impedance to, and thus acts indirectly on, the transmission network. The SVC functions as a controlled shunt reactive admittance that produces the required reactive compensating current. Thus, the attainable reactive compensating current is a function of the prevailing line voltage. It has been considered that the SVC is composed of TCR and TSC. Both TCR and TSC are controllable susceptances, and can therefore be applied as static compensators. As shown in Figure 1, the instantaneous current  $i$  of TCR is given by:

$$i = \begin{cases} \sqrt{2} \frac{E}{X_L} (\cos \alpha - \cos \omega t) & \alpha < \omega t < \alpha + \sigma \\ 0 & \alpha + \sigma < \omega t < \alpha + \Pi \end{cases} \quad (2)$$

Where  $V$  is the rms voltage,  $X_L = \omega L$  is the fundamental frequency reactance of the reactor;  $\omega = 2\pi f$ , and  $\alpha$  is the gating delay angle. The time origin is chosen to coincide with a positive-going zero-crossing of the voltage [33]. The fundamental component is found by Fourier analysis and is given by:

$$i_1 = \frac{\sigma - \sin \sigma}{\pi X_L} E \quad (3)$$

Where

$$E = \sqrt{2} E \sin \omega t \quad (4)$$

$\sigma$  is the conduction angle, related to  $\alpha$  by the equation

$$\alpha + \frac{\sigma}{2} = \Pi \quad (5)$$

We can write equation (3) as:

$$i_1 = B_L(\sigma)E \quad (6)$$

Frequency susceptance controlled by the conduction angle according to the law:

$$B_L(\sigma) = \frac{\sigma - \sin(\sigma)}{\pi X_L} \quad (7)$$

In TSC, as shown in Figure 2, for preventing impulse currents a little series inductance is added in circuit. The voltage equation in terms of Laplace transform is:

$$E(s) = \left[ Ls + \frac{1}{Cs} \right] i(s) + \frac{E_{C0}}{s} \quad (8)$$

The supply voltage is given by:

$$E = \hat{E} \sin(\omega_0 t + \alpha) \quad (9)$$

Time is measured from the first instant when a thyristor is gated, corresponding to the angle  $\alpha$  on the voltage wave. By straightforward transform manipulation and inverse transformation we get the instantaneous current:

$$i(t) = \sqrt{2}I_{ac} \cos(\omega_0 t + \alpha) - nB_c \left[ E_{C0} - \frac{n^2}{n^2-1} \hat{E} \sin \alpha \right] \sin(\omega_n t) - \sqrt{2}I_{ac} \cos \alpha \cos(\omega_n t) \quad (10)$$

Where  $\omega_n$  is the natural frequency of the system

$$\omega_n = \frac{1}{\sqrt{LC}} = n\omega_0, \quad n = \sqrt{\frac{X_C}{X_L}} \quad (11)$$

$n$  is the per-unit natural frequency. The current has a fundamental component  $i_{ac}$ . Which leads the supply voltage by  $\frac{\pi}{2}$  radians. Its amplitude  $\hat{i}_{ac}$  is given by:

$$B_c \frac{n^2}{n^2-1} \quad (12)$$

The necessary conditions for transient-free switching are:

$$\cos \alpha = 0 \quad (\text{ie } \sin \alpha = \pm 1) \quad (13)$$

$$E_{C0} = \pm \hat{E} \frac{n^2}{n^2-1} = \pm X_C \hat{i}_{ac} \quad (14)$$

With conditions (13),(14),  $i(t)$  from (10) is:

$$i(t) = \hat{i}_{ac} \cos(\omega_0 t + \alpha) \quad (15)$$

Thus the total susceptance of SVC is:

$$B_{SVC} = B_{TSC} - B_{TCR} = B_c \frac{n^2}{n^2-1} - B_L(\sigma) \quad (16)$$

## OPERATION OF SYSTEM DESIGN

From the schematic the operation is explained based on following conditions. When both source and load are constant the bus voltage remains constant. When source is changed and load is constant, the bus bar voltage remains constant. When source is constant and load is changed, the bus bar voltage remains constant. VSEN (Voltage Sensor) takes the error signal from the output point it multiplies with rms value through the gain (k) and it sends to the amplifier.

Based on the two capacitor connections the bus bar voltage is balanced. This operation comes under TSC open loop control. Another type of control is TCR closed loop control which is based on control circuit-4. This circuit is used to control the firing angles for the operation of TCR. Based on this TCR operation the bus bar voltage is balanced. The signal received from the sensor is given to the four control circuits. The power circuit, compensated circuit and control circuits are given below:

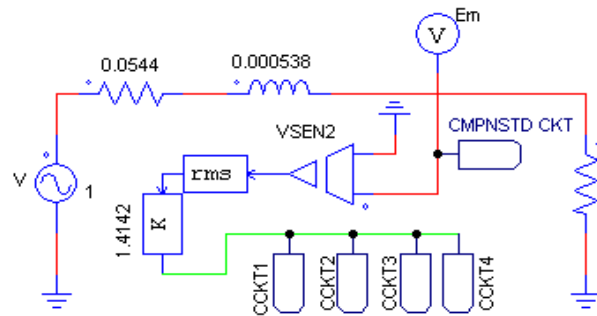


Figure 1: The Power Circuit

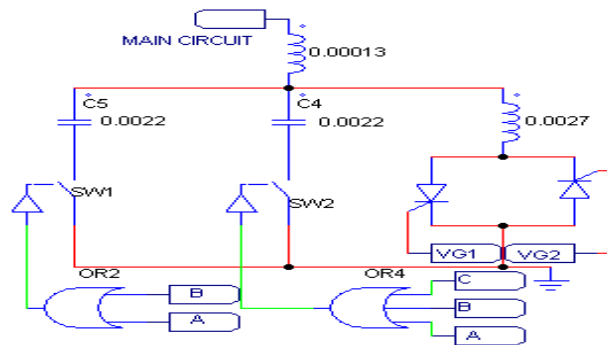


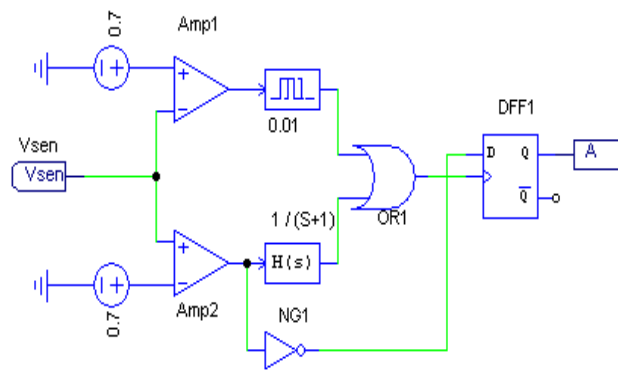
Figure 2: The Compensated Circuit

## Open Loop Control

### Control Circuit-1

The signal is sent to inverting amplifier-1, which is compared with the input assigned by the user. The output of the amplifier-1 is the difference between the assigned input and the signal received from the sensor. A delay circuit is used to transfer the constant output into variable output. This output is connected to OR-Gate 1 as final input. The 2<sup>nd</sup> input for OR-Gate 1 is connected from the actual input through the operational amplifier-2 with compensated gain. The purpose of this amplifier-2 is to differentiate the assigned input and signal sent.

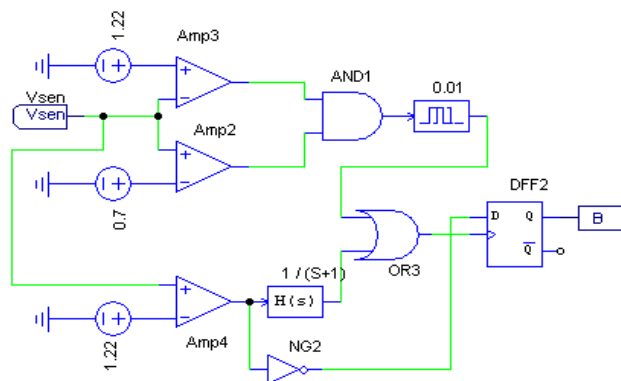
Finally, OR Gate 1 received one input from amplifier-1 through delay circuit and other input from amplifier-2 through compensated gain. So these two inputs are compared. From the two inputs of OR Gate, if any one input is 1, the output becomes 1 based on the truth table 1 of OR Gate. Based on the output (signal) from OR Gate-1 received the D flip flop will be operated. The purpose of D-flip flop is transfer the data without any change: When clock pulse is 0, no data will be transferred and When the clock pulse is 1, the input received by D-flip flop (i.e. 0 or 1) will be fully transferred to the OR Gate-2. The input for D-flip flop through NOT Gate. The purpose of NOT Gate is, the output received by amplifier-2 is 0, it transfers as 1 and if it is 1, it transfers as 0. The final output of D-flip flop is given as one output to OR Gate-2.



**Figure 3: Control Circuit-1**

### Control Circuit-2

The actual output signal from the sensor is given to the amplifier-3. The output received from amplifier-2 and the differential output from amplifier-3 are given as inputs to the AND Gate. The two inputs of AND Gate-1 are 1, the output will be 1. If anyone input is 0, the output becomes 0. This will be analyzed based on truth table of AND Gate. The first input for OR Gate-3 is received from amplifier-2 and 3 through the delay circuit based on AND Gate. The second input is received from the differential output of amplifier-4 through the compensated gain. The input for amplifier-4 is from actual output signal from the sensor and the input signal assigned by the user. From the two inputs of OR Gate-3, if any one input is 1, the output becomes 1 based on the truth table 1 of OR Gate. Based on the output (signal) from OR Gate-3 received, the D flip flop will be operated. The purpose of D-flip flop is transfer the data without any change: When clock pulse is 0, no date will be transferred and When the clock pulse is 1, the input received by D-flip flop (i.e. 0 or 1) will be fully transferred to the OR Gate-2 and 4. The input for D-flip flop is through NOT Gate. The purpose of NOT Gate is, the output received by amplifier-4 is 0, it transfers as 1 and if it is 1, it transfers as 0. The final output of D-flip flop is given as one output to OR Gate-2 and 4.



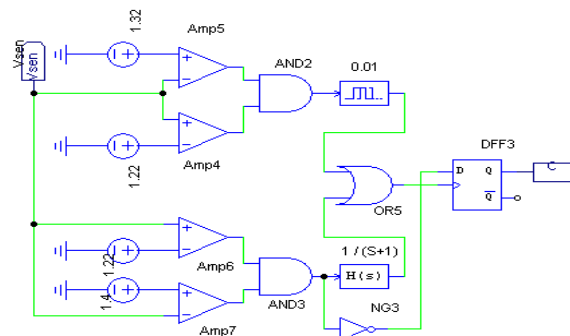
**Figure 4: Control Circuit-2**

### Control Circuit-3

The actual output signal from the sensor is given to the amplifier-3. The output received from amplifier-2 and the differential output from amplifier-3 are given as inputs to the AND Gate. The two inputs of AND Gate-1 are 1, the output will be 1. If anyone input is 0, the output becomes 0. This will be analyzed based on truth table of AND Gate. The first input for OR Gate-5 is received from amplifier-4 and 5 through the delay circuit based on AND Gate operation.

The second input is received from the amplifier-6 and 7 through the compensated gain based on AND Gate operation. The inputs for amplifier-4, 5, 6 and 7 is from the actual output signal from the sensor and the input signal assigned by the user on his requirement. From the two inputs of OR Gate-5, if any one input is 1, the output becomes 1 based on the truth table 1 of OR Gate. Based on the output (signal) from OR Gate-5 received, the D flip flop will be operated. The purpose of D-flip flop is transfer the data without any change: When clock pulse is 0, no data will be transferred and When the clock pulse is 1, the input received by D-flip flop (i.e. 0 or 1) will be fully transferred to the OR Gate-2 and 4. The input for D-flip flop is through NOT Gate. The purpose of NOT Gate is, the output received by amplifier-6 and 7 through AND Gate is 0, it transfers as 1 and if it is 1, it transfers as 0. The final output of D-flip flop is given as one output to OR Gate-2 and 4.

Based on the outputs of OR Gate-2 and 4 and ON and OFF switches (two) in the schematic are operated. The switch-1 operation is based on OR Gate-2 and the switch-2 operation is based on OR Gate-4. The total control of the switch-1 is based on the control circuit- 1 and 2 through OR Gate-2. The control of switch-2 is based on the control circuit-1, 2 and 3 through OR Gate-4. This switch-1 is used to connect the capacitor (C1) with the system. And switch-2 is used to connect the capacitor (C2) with the system. Based on these two capacitor connections the bus bar voltage is balanced. This operation comes under TSC open loop control. Another type of control is TCR closed loop control which is based on control circuit-4. This circuit is used to control the firing angles for the operation of TCR. Based on this TCR operation the bus bar voltage is balanced.



**Figure 5: Control Circuit-3**

## Closed Loop Control

### Control Circuit-4

The actual output signal from the sensor is given as one input to the amplifier-8 and 9 through the summer-1. The purpose of summer-1 is comparing the actual output signal from sensor and the input assigned by the user. The outputs of the amplifier-8 and amplifier-9 are based on the inputs given. The outputs of amplifier-8 and 9 are given to the summer-2 through the required compensated gains. The output of summer-2 is given to the summer-3. Summer-3 compares this signal with the input assigned by the user. The output of summer-3 is given to summer-4 through a limiter. The purpose of this limiter is keep the output of summer-3 within the limits. The output of summer-4 is compared with the input assigned by the user and given to alpha controller-2. The input of the alpha controller-1 is received from the limiter. The other input sources of alpha controllers are commonly received from square and dc. The outputs of the alpha controllers are given to the gate terminals present in the TCR device. Based on these alpha controllers the TCR is operated and the bus bar voltage is balanced.

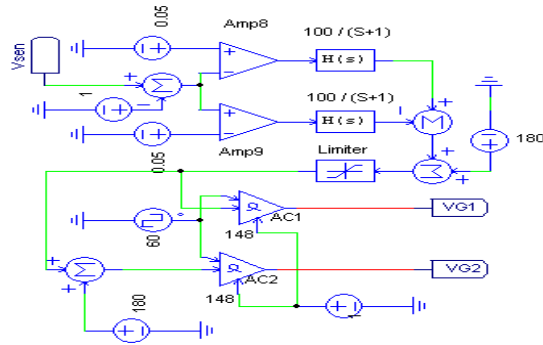


Figure 6: Control Circuit-4

## RESULTS AND DISCUSSIONS

The designed system with SVC control that is simulated with psim software. The simulation results in three conditions are considered. The simulation results of bus bar voltage and firing angle of TCR and on or off states of two capacitors are shown below:

- $V = 1$  pu and  $R_{load} = 1$  pu
- $V = 0.9167$  pu and  $R_{load} = 1$  pu
- $V = 1$  pu and  $R_{load} = \infty$

In case (a), as shown in Figure 7 & 8, the bus bar voltage ( $E_m$ ), reaches to the desired value of 1pu, and the capacitor C1 is on and C2 is off, and the firing angle ( $\alpha$ ) is about  $148^\circ$ .

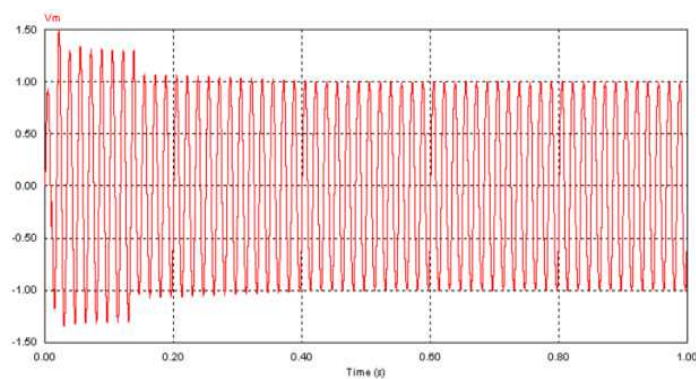


Figure 7: Bus Bar Voltage (a)

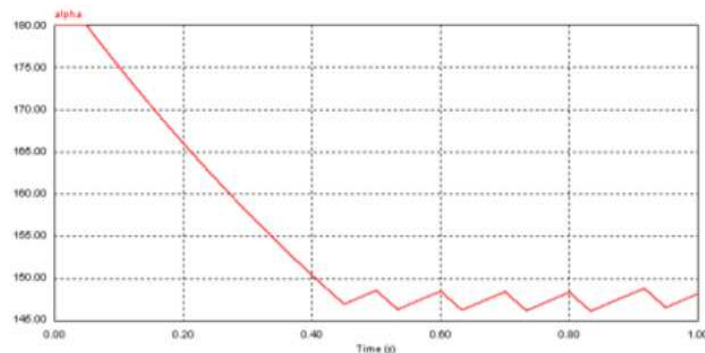
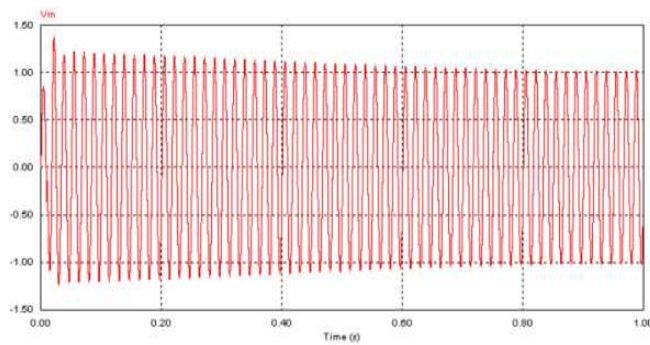
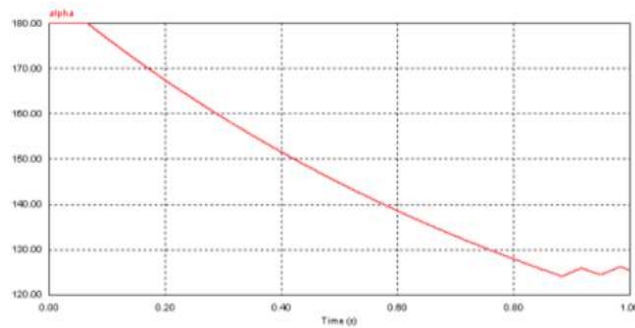


Figure 8: Firing Angle  $\alpha$  in Degrees (a)

In case (b), as shown in Figure 9 & 10, the bus bar voltage ( $E_m$ ), reaches to the 1pu very slowly, compared with the case (a), and both C1, C2 are on, and firing angle slowly reaches to the value of about  $125^\circ$ .

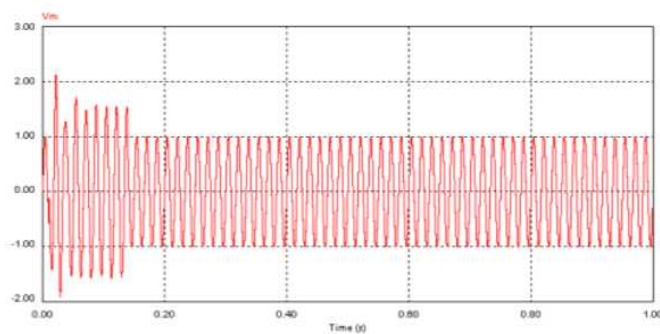


**Figure 9: Bus Bar Voltage (b)**

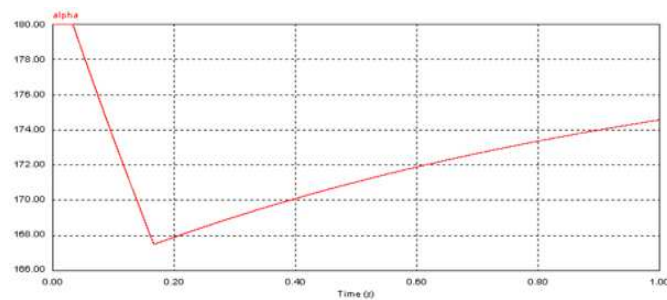


**Figure 10: Firing Angle  $\alpha$  in Degrees (b)**

In case (c), as shown in Figure 11 & 12, the bus bar voltage reaches to 1pu and both capacitors C1, C2 are off and firing angle slowly reaches to the value of  $176^\circ$ .



**Figure 11: Bus Bar Voltage (c)**



**Figure 12: Firing Angle  $\alpha$  in Degrees(c)**



**Observation Results:** The following results are obtained from the system design based on the three conditions:

**Table 1: Observation Results**

Sl. No.	Results	Source Voltage ( $V_s$ ) in pu	Load (R) in pu	Bus Bar Voltage ( $E_m$ )	Firing Angle ( $\alpha$ )	Capacitor Voltage ( $V_{C1}$ )	Capacitor Voltage ( $V_{C2}$ )
1	Case (a): Source and load are constant	1	1	Desired value 1 pu	$148^\circ$	1 pu	0
2	Case (b): Changing of source and constant load	0.9167	1	Nearly 1 pu	$125^\circ$	1 pu	1 pu
3	Case (c): Changing of load and constant source	1	$\infty$	Equal to 1 pu	$176^\circ$	0	0

## CONCLUSIONS

In designed system only one voltage sensor (PT) has been used, and that is sufficient for maintaining voltage stability in the bus bar. As the simulations show, this new control strategy is operating effectively. Simulation of the system with PSIM software shows that this control method for the limits of  $0.81\text{pu} < V < 1.14\text{pu}$  and  $R \geq 0.6\text{pu}$ , is operating effectively and maintain  $E_m$ , very close to the value of 1 pu. Low costing and simplicity are the advantages of this control method in practice. The design system is operated based on four control strategies. In this three control strategies (1, 2 & 3) are operated as open loop control and the fourth control strategy is operated as closed loop control. The control strategies involve the combination of components like logic gates, flip flops, delay circuits, compensated gains, and op-amps. Based on these control strategies the bus bar voltage is balanced.

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